

CES-SDT base configuration short-form data

General

This programmable hardware block performs AAL1 circuit emulation inter-working functions for structured data transfer (SDT). It is one of a number of interworking functions, which use Phystream's new communications processing architecture, which is scalable, configurable and fully customizable for a range of data access applications.

Numbers of channels can be scaled up for higher density applications, or scaled down for cost effective low bandwidth designs. The function is configurable to enable maximum flexibility in protocol operation, and is customisable to Customer specification for any interfacing requirement.

Features

- 63 x E1
- 256 channels
- Flexible allocation of timeslots to VCs
- Trunk conditioning on a per timeslot basis
- Transparent transmission of Common Channel Signalling (CCS)
- Two external 32-bit memory devices
- Flexible memory allocation for CDV buffering
 - Supports zero CDVT for low latency applications
 - Maximum CDV buffer size limited only by external memory capacity
- UTOPIA Level 1 interface
- TDM interface to Customer specification
- Generic 32-bit processor interface
- Programmable ATM cell header
- Flexible channel identification (e.g. VPI/VCI, routing tag, etc.)
- Fast sequence number processing algorithm
- Low latency access for statistics
- Compliant with ITU I.363.1, ATMF af-phy-0017.000 UTOPIA Level 1 version 2.01, ATMF af-vtoa-0078.000 version 2.0 CES Interoperability Specification
- Flexible clocking strategies
 - Single global clock, or
 - Individual interface clocks

Minimum Requirements

XC2V1000-4 FPGA

32 bit, 64Mbit SDRAM

32 bit, 128Kbit SSRAM

System clock frequency: 25MHz (min)

Options

- Increased channel capacity
- Support for Channel Associated Signalling (CAS)
- Partial cell fill for delay sensitive applications
- Combination with Phystream AAL1-UDT IP
- Dynamic Bandwidth CES (DBCES) af-vtoa-0085.000
- Adaptive sequence number processing algorithm
- UTOPIA Level 2 interface af-phy-0039.000
- System and line loop-back on a connection basis
- PRBS test generation/detection
- Forward compatibility with Phystream's IWF portfolio

Applications

SDT is the type of circuit emulation service (CES) most suitable for provision of narrowband voice, leased line and digital cross connect applications.

The Phystream SDT package is designed to accommodate all these applications with unprecedented efficiency, allowing state-of-the-art density of channelization when used in conjunction with available 3rd party framing devices, as shown:

