

Phystream Limited

22 Elm Way, Melbourn,
 Royston, Herts
 United Kingdom, SG8 6UH
 Phone: +44 (0)20 8469 4019
 E-mail: query@phystream.com
 URL: www.phystream.com

Features

- Complies with ATMF Inverse Multiplexing for ATM (IMA) version 1.1, af-phy-0086.001
- Supports up to 84 TDM links
- Supports up to 84 IMA groups
- Supports any frame size, M=32, 64, 128 (default) or 256 within each IMA group
- Supports independent (ITC) and common (CTC) clock modes for each IMA group
- Flexible connection to required Delay Compensation Buffer (DCB), either internal block RAM or external memory
- Fully supports IMA-MIB
- Efficient co-processing architecture, using Phystream phyCore combined with either immersed MicroBlaze, PowerPC or discrete processor
- Verilog source for the IMA convergence IP module
- C++ source for IMA application software
- Glue-less interface to Phystream ATM Transmission Convergence IP module
- Compatible physical interface products available from Phystream
- Simple integration through software interface
- Available under terms of the SignOnce IP License

Core Facts	
Provided with Core	
Documentation	User Guide
Design File Formats	NGC, Verilog, VHDL, C++ source
Constraints Files	abel.ucf
Verification	Test Bench, Test Vectors
Instantiation templates	VHDL, Verilog
Reference designs & application notes	Reference designs available for MicroBlaze and PowerPC
Additional Items	phySim simulator for phyCore, ATM TC and interface IP
Verification	
Phystream phySim, PPC405 ISS 1.4 (1.68), MicroBlaze ISS (EDK 6.2), Modeltech modelsim 5.7g, Virtex and Virtex-II Pro hardware development systems	
Support	
Support provided by Phystream Limited	

Table 1: Example Implementation Statistics for IMA-4 (IMA convergence only, see Figure 1)

Family	Example Device	Fmax (MHz)	Slices ¹	GCLK	BRAM	MULT	DCM/DLL	MGT	PPC	Design Tools
Spartan-3™	XC3S50-4	100	499	1	1	0	0	0	0	ISE 6.2.03i
Virtex-II Pro™	XC2VP4-5	100	499	1	1	0	0	0	0	ISE 6.2.03i
Virtex-II™	XC2V80-5	100	499	1	1	0	0	0	0	ISE 6.2.03i
Virtex-4™	XC4VLX15	100	510	1	1	0	0	0	0	ISE 6.3.01i

Notes:

1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details

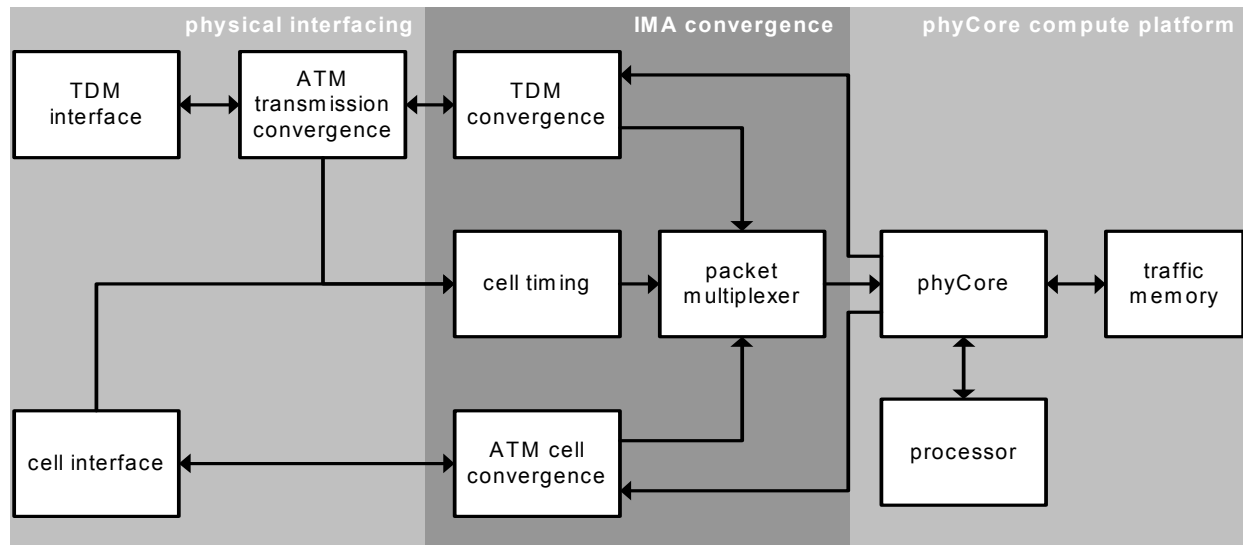


Figure 1: Inverse Multiplexing over ATM for phyCore Block Diagram

Applications

The IMA for phyCore solution can address a number of different applications due to the exceptional scalability of the solution. This scalability comes from the concentration of functionality in software, and the flexibility to choose the appropriate processor type for the application.

Integrated access devices (IAD) may require a small number of links to be supported. IMA for phyCore can be deployed with a MicroBlaze processor or discrete processor, targeted at a low-cost Spartan3 device. The MicroBlaze solution provides a self-contained, scalable solution for low-bandwidth applications. Alternatively, spare processing power on the host system processor can be used to provide the computing power required to run the IMA application software.

High capacity edge switches and DSLAMs require higher bandwidth termination. The use of the immersed PowerPC within Virtex-II Pro devices provides a highly integrated high-bandwidth solution. A single processor can support 32 TDM links, with sufficient additional computing resource for higher layer functions. By concentrating more of the datapath functions on a single device, more efficient use of subsystem components is achieved. This results in reduced memory and associated logic, fewer physical interfaces and reduced interconnect, reduced power, a simpler control architecture and an inherently more scalable design.

The IMA for phyCore can be combined with other Phystream applications, for use in multi-service access equipment. Since the IMA application is delivered in source formats, the application can easily be modified for combination with the customer's own intellectual property. This allows the addition of different physical interfaces (telecom bus, POS-PHY, proprietary etc.), datapath modules (encryption, packet classification etc.) or application software (packet forwarding, control plane, etc.).

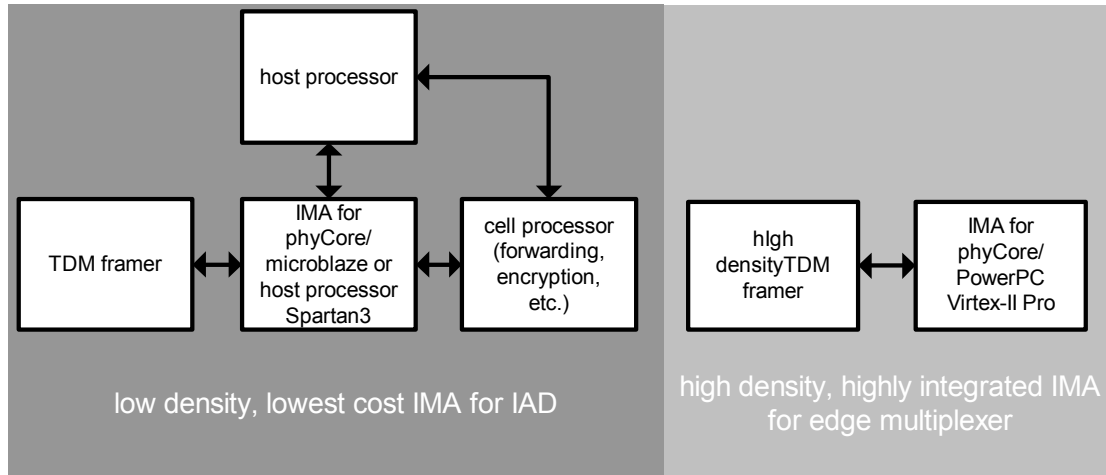


Figure 2: Example Applications

General Description

IMA for phyCore is a hardware/software co-processing implementation of Inverse Multiplexing over ATM. IMA provides a means of combining low-speed ATM links to give the characteristics of a proportionately higher speed interface. IMA for phyCore provides a uniquely scalable solution when combined with an appropriate phyCore dataflow processor, covering the full spectrum of IMA applications from low cost Customer Premises Equipment to high capacity edge switches and DSLAMs.

The application is delivered as Verilog source for the hardware portion, and C++ source code for the application software, for easiest integration and modification.

Functional Description

TDM Convergence

The TDM Convergence block accepts ATM cells from the ATM transmission convergence block. These cells are classified in order to discriminate between user cells and OAM cells. The ATM HEC is discarded once it has been checked. A status word is added to the encapsulation data which precedes the cell. This phyCore encapsulation accelerates downstream processing of the cell stream by determining which cells require further processing. In addition, the phyCore encapsulation indicates the input queue for each cell. The input queues are used to provide delay compensation buffering (DCB).

Encapsulated cells received from phyCore have the phyCore encapsulation removed and processed. IMA OAM cells have a CRC-10 calculated and inserted. A HEC is calculated and inserted for each output cell.

ATM Cell Convergence

The ATM Cell Convergence block encapsulates ATM cells for phyCore. This involves adding the identity of the input queue. Encapsulated cells received from phyCore have the phyCore encapsulation removed.

Cell Timing

The physical interfaces are responsible for requesting cells for their ports. A TDM interface request might be triggered by a low watermark being reached on a TDM buffer. The cell rate of ports on the cell

interface is determined by the IMA data clock, which in turn is related to the number of active links within an IMA group, and the rate of the timing reference link (TRL) within each group.

Cell requests are presented at a request interface. These consist of a queue identifier that is associated with the requesting port, a free queue identifier where the freed buffer can be returned, and a strobe. The Cell Timing block stores requests, and formats these into command packets that are sent periodically to the Packet Multiplexer.

Packet Multiplexer

The Packet Multiplexer accepts data packets from the Convergence blocks, and command packets from the Cell Timing block, and presents these to phyCore. The Packet Multiplexer polls each of the Packet Sources for packets, and manages the flow of packets between the interfaces and phyCore.

ATM Transmission Convergence

The ATM Transmission Convergence block is not part of the IMA for phyCore application. It is available as a separate IP block. It provides bulk cell delineation, HEC checking, payload scrambling and descrambling, header error correction and cell filtering.

The ATM Transmission Convergence block is responsible for requesting egress ATM cells from phyCore. A request consists of a queue identifier associated with a TDM port that requires more data.

TDM Interface

The TDM Interface is not part of the IMA for phyCore application. In the example of Figure 1, the TDM interface provides physical connection to a TDM framer device, and timeslot discrimination. This function is available as a separate IP block.

An alternate configuration would be to connect an ATM UNI device directly to the IMA Convergence block. This is most suitable when there are only ATM UNI links connected to the equipment i.e. no voice or packet data.

Cell Interface

The Cell Interface provides the system interface. The implementation would depend on the requirements of the downstream components. An example is a UTOPIA level 2 interface, which is available as a separate IP block from Phystream.

The Cell Interface must provide cell flow control in both directions. In the egress direction, the cell rate for each port must be controlled to match the transmit IMA data cell rate (IDCR) for the corresponding IMA group. This rate varies depending on the number of operational links within the IMA group. The IMA application software provides device driver calls to adjust the transmit cell rate accordingly. The Cell Interface is responsible for translating these driver calls into physical flow control signals. The Phystream UTOPIA L2 IP module provides a cell rate controller that can be programmed to an accuracy of greater than 50ppm. For the ingress direction, the receive IMA data cell rate is used to generate cell requests for ATM cells for phyCore.

PhyCore

PhyCore consists of a hardware netlist and a C interface library. The phyCore subsystem acts as a hardware operating system. It creates software tasks that map directly to state changes within the

queuing system, and presents these tasks to the software subsystem in a format that requires no further processing. It accepts commands from both hardware and software datapaths, to move data through the queuing system, access or modify the data. Communication between phyCore hardware and software library is extremely efficient, effectively removing the bottleneck of conventional bus-based system, and greatly increasing the throughput of the system.

The hardware netlist provides physical interfacing (POS-PHY Level 3), autonomous queuing, direct memory access (DMA) and queue event/command translation. A memory controller is required to interface phyCore to a suitable traffic memory system. For low-bandwidth applications, this might be a block RAM controller and BRAM memory. Higher bandwidth requirements may require the use of external SDRAM or SRAM.

The phyCore software library provides low-level interfacing to the phyCore hardware, command (DMA and queue) and event interfaces for access to the underlying traffic data, and a debug interface. The simple API makes phyCore easy to use. The debug interface provides real-time instrumentation of the code, allowing the application to be traced during normal operation.

PhySim is a simulation environment for the development of system models, hardware and software. It provides high-speed simulation environment that can operate on a desktop PC, target processor instruction set simulator or target hardware. PhySim can be used to accelerate the integration of IMA for phyCore within the target system software environment.

Processor

The choice of companion processor for phyCore can be made to trade off cost, performance and level of integration. Immersed Xilinx MicroBlaze and PowerPC are currently supported. For support of other processor architectures contact Phystream.

Traffic Memory

The traffic memory subsystem consists of a memory controller and memory. The link density and required delay compensation determine the size of the memory required, and hence whether internal or external memory is required. IMA for phyCore is capable of passing more than 300Mb/s with standard SDRAM technology.

IMA Application Software

The bulk of the IMA sub-layer in the IMA for phyCore application is implemented in software. Operation is independent of the host system. Interaction with IMA for phyCore is only required to modify configuration, and to retrieve statistics.

The application is written in C++, and is available in source code form. This allows easy extension, and integration with other software functions.

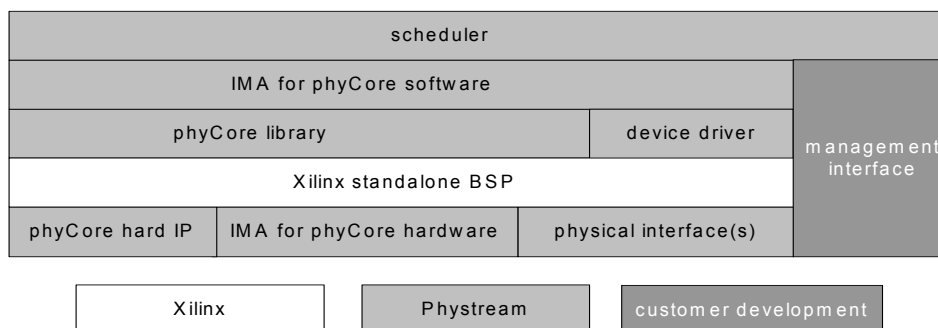


Figure 3: IMA Application Block Diagram

Core Modifications

The IMA for phyCore application is provided as Verilog and C++ source code. Both the hardware and software modules are available for customer modification.

Verification Methods

The IMA for phyCore application has been tested by simulation on the Phystream phySim simulator (desktop, MicroBlaze ISS and PPC405 ISS). Hardware interfaces have been tested using the phyCore bus functional model (BFM) on modelsim 5.7g, with test vectors generated by the IMA application running on phySim. IMA for phyCore has also been verified on hardware development systems for both MicroBlaze and PowerPC variants.

Recommended Design Experience

Knowledge of HDL design and C/C++ software design is required to modify and integrate IMA for phyCore into a customer design. Phystream can also undertake the integration activity to provide a complete turnkey solution.

Available Support Products

Phystream's phySim is a very high-speed simulator, used for the development of phyCore-based hardware/software subsystems. This product can be used to accelerate the development of extensions to the base product.

Phystream provide a range of physical interface IP blocks that can be combined with IMA for phyCore to provide a complete IMA subsystem.

Ordering Information

This product is available directly from Phystream under the terms of the SignOnce IP License. Please contact Phystream for pricing and additional information about this product. Contact information for Phystream is on the front page of this datasheet. To learn more about the SignOnce IP License program, contact Phystream or visit the web:

Email: commonlicense@xilinx.com
URL: www.xilinx.com/ipcenter/signonce

Related Information

Industry Information

The Inverse Multiplexing for ATM (IMA) Specification Version 1.1 AF-PHY-0086.001 is available from the ATM Forum at www.atmforum.com.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com