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Features

- Supports up to 64 independent cell streams
- Supports cell rate of 285 kcells in each direction
- Conforms to I.432, af-phy.0064.000, af-phy.0043.000, af-phy.0016.000
- Cell Delineation state machine for configurable number of cell streams
- Configurable single bit header correction
- Configurable payload scrambling and descrambling
- Loss of Cell Delineation (LCD) state machine
- Programmable receive cell filter per port
- Port statistics interface
- Suitable as an IMA interface-specific transmission convergence sublayer : no cell discard, no cell rate decoupling, additional cell delineation state and error status outputs
- Compatible with Phystream IMA for phyCore co-processing IP
- Compatible with Phystream Programmable TDM (framer) Interface IP
- DCR (Device Control Register) Interface for configuration
- Available under terms of the SignOnce IP License

Core Facts	
Provided with Core	
Documentation	User Guide
Design File Formats	NGC
Constraints Files	atmtc.ucf
Verification	Test Bench, Test Vectors
Instantiation templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
Modeltech modelsim 5.7g	
Support	
Support provided by Phystream Limited	

Table 1: Example Implementation Statistics for ATMTTC (64 links)

Family	Example Device	Fmax (MHz)	Slices ¹	IOB ²	GCLK	BRAM	MULT	DCM/DLL	MGT	PPC	Design Tools
Spartan-3™	XC3S400-4	100	565	260	2	5	0	0	N/A	N/A	ISE 6.2.03i
Virtex-II Pro™	XC2VP4-5	100	565	260	2	5	0	0	0	0	ISE 6.2.03i

0

Notes:

1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details

2) Assuming all core I/Os and clocks are routed off-chip

0.1

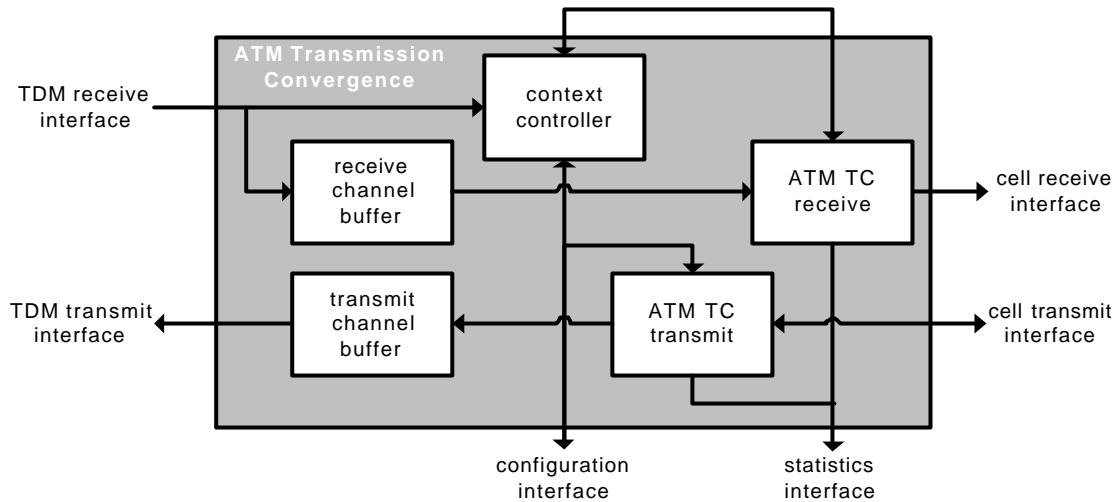


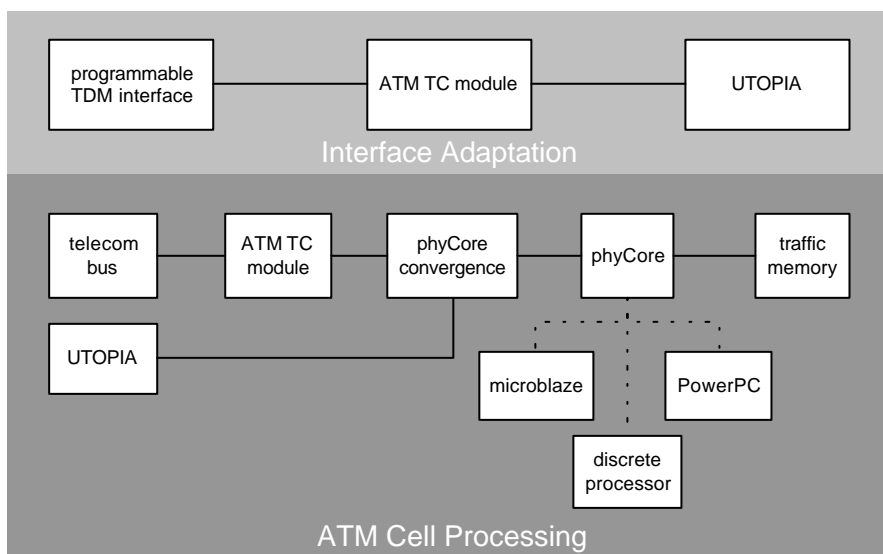
Figure 1: ATM Transmission Convergence Block Diagram

Applications

The Phystream ATM Transmission Convergence IP module employs an efficient context-switched architecture that makes it suitable for both low and high-density applications. The TDM and cell interfaces can be easily adapted to integrate into the target environment. Typical applications include:

- Integrated Access Devices (IAD)
- Digital Subscriber Line Access Multiplexers (DSLAM)
- ATM access equipment
- Inverse Multiplexing over ATM (ATM)

The ATM TC module can be deployed as a standalone IP block, for combination with customer IP or Phystream interface modules for a variety of interfacing applications. Alternatively, ATM TC can be combined with the phyCore Dataflow Processor to produce a powerful and flexible ATM Cell Processor. PhyCore can employ immersed PowerPC or microblaze processors as the compute platform, or an external processor.



General Description

The ATM Transmission Convergence module extracts cells from a set of incoming TDM data streams. Complete cells are presented at the cell receive interface. A programmable, per port, cell filter can be used to filter certain cell types. Payload descrambling and single bit cell header error correction can be programmed on a per port basis.

In the transmit direction, The ATM TC transmit module requests cell from the upstream interface as required. The cell payload can be configured, on a per port basis, for scrambling. The TDM transmit interface requests timeslots as required. When cell data is not available a trunk-conditioning pattern is sent.

Functional Description

Receive Channel Buffer

The Receive Channel Buffer is used to assemble cells prior to processing by the ATM TC receive module. The TDM interface indicates the presence of a new timeslot, the identity of the associated tributary and the timeslot data. A set of FIFOs is maintained in the Receive Channel Buffer for each tributary. The read and write processes for the Receive Channel Buffer are controlled by the context controller.

Context Controller

The Context Controller monitors the Receive Channel Buffer FIFO status. When there is sufficient data within a tributary FIFO, the associated context is loaded and the data presented to the ATM TC receive module for processing. Once cell processing is complete, the ATM TC receive context is stored.

ATM TC Receive

The ATM TC Receive module runs a cell delineation state machine for each incoming cell stream. Cell boundaries are identified, and recovered cells are presented at the cell receive interface. The ATM header of each cell is compared against a programmed filter value and a match output is generated. The filter is specified at logic one, zero or don't care in each bit position. The cell delineation state and HEC error status for each cell is also presented. All cells are available at the cell interface, and discard can be performed based on the filter and state machine states. This allows the ATM TC module to be used for IMA applications where all cells must be presented to the ATM sub-layer, including errored cells.

The following ATM TC Receive parameters, for each port, can be configured over the DCR control interface:

- Single header error correction
- Cell payload descrambling
- Cell delineation state machine ALPHA and DELTA thresholds
- Cell filter specification

ATM TC Transmit

The ATM TC Transmit module is responsible for transferring cell data from the cell interface, to the TDM interface, on demand from the TDM interface. The TDM interface requests a TDM timeslot by specifying a tributary identifier. The next cell data timeslot is presented at the TDM transmit interface at a fixed latency. The timeslot is then replaced in the Transmit Channel Buffer by reading the next cell octet over the Cell Transmit interface. The behaviour of this interface is simply that of a block RAM read-only port. Payload octets are optionally scrambled prior to writing to the Transmit Channel Buffer. If there is no cell data available, a trunk-conditioning pattern is written into the Transmit Channel Buffer.

When the start of a cell is processed, another cell is requested upstream. The format of this request is compatible with the phyCore dataflow processor. It identifies the tributary, which requires more data. The upstream datapath has one cell period to supply the requested cell, else trunk conditioning is performed. The downstream interface presents cells in through a two buffer FIFO per tributary. One location within each

buffer pair is used to indicate the current write buffer. This information is used by the ATM TC Transmit interface for synchronization, and detection of underflow.

The following ATM TC Transmit parameters, for each port, can be configured over the DCR control interface:

- Cell payload scrambling

Transmit Channel Buffer

The Transmit Channel Buffer provides a low latency buffer for servicing TDM timeslot requests from the TDM transmit interface. A single octet is stored for each tributary. The ATM TC transmit module is responsible for controlling transfer of octets from the cell transmit interface to the Transmit Channel Buffer.

Core Modifications

The ATM TC module is supplied as a Xilinx NGC netlist. Verilog source code can be purchased for user customization. Alternatively, Phystream can undertake customization of the core as required.

Verification Methods

The ATM TC module has been tested in simulation using modelsim 5.7g, and on a Virtex-E development platform.

Recommended Design Experience

Knowledge of HDL design and Xilinx tools is recommended for use of this core. Knowledge of ATM systems would also be useful.

Available Support Products

Phystream provide a range of physical interface IP blocks that can be combined with the ATM TC module. The Phystream Programmable TDM interface provides serial interfacing for low to medium density applications. ATM Convergence for phyCore provides the necessary interfacing to connect the ATM TC module to the phyCore dataflow processor. This provides a platform for a range of ATM cell processing functions, including traffic management and OAM processing.

Ordering Information

This product is available directly from Phystream under the terms of the SignOnce IP License. Please contact Phystream for pricing and additional information about this product. Contact information for Phystream is on the front page of this datasheet. To learn more about the SignOnce IP License program, contact Phystream or visit the web:

Email: commonlicense@xilinx.com
URL: www.xilinx.com/ipcenter/signonce

Related Information

Industry Information

The following specifications are available from The ATM Forum at www.atmforum.com:

- DS1 Physical Layer Specification af-phy-0016.000
- E1 Physical Interface Specification af-phy-0064.000
- A Cell-Based Transmission Convergence Sublayer for Clear Channel Interfaces af-phy-0043.000

The specification "B-ISDN User-Network Interface: Physical Layer Specification", ITU-T I.432, is available from the International Telecommunication Union at www.itu.int.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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