



Multi-port Serial-UTOPIA Bridge

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Product Specification

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Features

- Supports 1-8 physical ports
- Programmable TDM interface
 - Clock, data and sync for connection to most DS1/E1 or DSL framers
 - Programmable frame format
 - Master and slave operation
- ATM Transmission Convergence
 - Conforms to I.432, af-phy.0064.000, af-phy.0043.000, af-phy.0016.000
 - Cell Delineation
 - Configurable single bit header correction
 - Configurable payload scrambling
 - Loss of Cell Delineation (LCD) state machine
 - Programmable receive cell filter per port
 - Programmable transmit cell rate decoupling cell definition per port
- UTOPIA Level 2 PHY interface
 - Conforms to af-phy-0039.000
 - Cell or octet-level handshake

Core Facts	
Provided with Core	
Documentation	User Guide
Design File Formats	Xilinx NGC netlist
Constraints Files	barley_wrapper.ucf
Verification	Test Bench, Test Vectors
Instantiation templates	VHDL, Verilog
Reference designs & application notes	
Additional Items	C Driver Code
Simulation Tool Used	
Modeltech Modelsim v5.8	
Support	
Support provided by Phystream Ltd	

- 8-bit data
- Comprehensive port and interface statistics
- DCR (Device Control Register) Interface
 - Configuration and control
 - Access to interface and port statistics counters
- Available under terms of the SignOnce IP License
- Optimized for Spartan-3

Table 1: Example Implementation Statistics for 1-Port Configuration

Family	Example Device	Fmax (MHz)	Slices ¹	IOB ²	GCLK	BRAM	MULT	DCM/DLL	MGT	PPC	Design Tools
Spartan-3™	XC3S50-4	50	766	89	1	4	0	0	N/A	N/A	ISE 6.1.03i

Table 2: Example Implementation Statistics for 8-Port Configuration

Family	Example Device	Fmax (MHz)	Slices ¹	IOB ²	GCLK	BRAM	MULT	DCM/DLL	MGT	PPC	Design Tools
Spartan-3™	XC3S200-4	50	1409	145	1	5	0	0	N/A	N/A	ISE 6.1.03i

Notes:

1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details

2) Assuming all core I/Os and clocks are routed off-chip

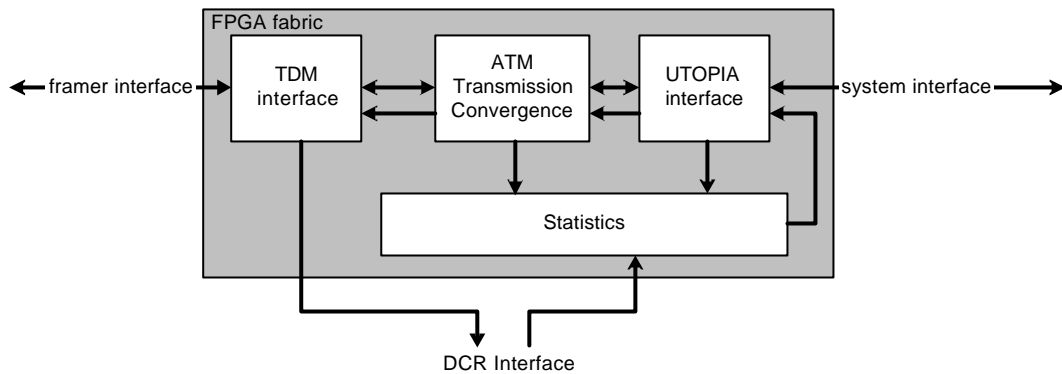


Figure 1: Multi-port Serial-UTOPIA Bridge Block Diagram

Applications

- Multi-service access platforms
- Integrated Access Devices (IADs)
- ATM User to Network Interfaces (UNIs)
- Standard Hardware platforms

General Description

The Serial-UTOPIA Bridge integrates ATM transmission convergence functions with appropriate datapath and control interfaces. When combined with a standard DS1/E1 or DSL framer, the module provides a flexible, high density, and low cost alternative to conventional ATM PHY layer devices.

The TDM interface provides flexible serial interfacing. Cells are extracted from the ingress octet stream by the Receive ATM TC function. Single bit header errors can be corrected. A programmable cell filter allows PHY and/or ATM layer Unassigned cells to be filtered. Cell rate decoupling is provided in the transmit direction, with each port having a programmable cell definition. The UTOPIA interface provides standard UTOPIA Level 2 slave functionality, including both cell and octet level handshaking. Statistics are collected centrally, and are accessible through the Device Control Register (DCR) interface.

Functional Description

TDM Interface

In the ingress direction, the TDM interface extracts octets from the receive serial interface. The format of the receive TDM frame is programmable. This allows the receive frame pulse position, receive frame length and receive octet mapping (channelization) to be dynamically configured. In addition, frame synchronization can be to either an external, or internal, framing signal. Accepted octets are written into a per-port channel buffer.

In the egress direction, the TDM interface transfers octets from a per-port channel buffer to the transmit serial interface. The transmit frame format is programmable. This allows the transmit frame pulse position, transmit frame length and transmit octet mapping (channelization) to be dynamically configured. As with the receive port, frame synchronization can be sourced or sinked.

Each TDM port is fully independent from the other ports. In addition, the transmit and receive sections of each TDM port are also independent.

ATM Transmission Convergence

The ATM Transmission Convergence (TC) block extracts ATM cells from a continuous receive cell stream, and multiplexes ATM layer cells and cell rate decoupling cells to produce a continuous transmit cell stream.

The ATM TC module implements the cell delineation state machine of I.432.1 in order to determine cell boundaries, and thereby extract incoming cells. The TC function can be programmed (per-port) to correct single-bit header errors. Corrected cells are presented to a per-port cell filter. The filter compares each ATM header against a programmable filter definition. Each bit position can be specified as one, zero or don't care. ATM cell payloads can be optionally descrambled, as described in I.432.1. Accepted cells are written into the ingress UTOPIA buffer.

In the egress direction, the ATM TC module transfers octets from either the egress UTOPIA buffer, or per-port cell rate decoupling cell buffer. When there is no ATM layer cell available for a particular port, a cell rate decoupling cell is inserted. The format of this cell can be programmed for each port. Each port can be programmed for cell payload scrambling.

UTOPIA Interface

The UTOPIA interface provides an 8-bit UTOPIA PHY layer (slave) interface, as specified in ATMF af-phy-0039.000, operating up to 50MHz. The interface can be configured for multi-device (tristate multiplex) or single device (direction connection). Each UTOPIA transmit PHY has a programmable enable.

Statistics

The statistics module gathers port and interface statistics for presentation to the DCR control interface. The following statistics are collected as 16 bit rollover counts for each serial port:

- Received cells
- Transmitted cells
- Uncorrected ATM header errors
- Corrected single bit ATM header errors
- Loss of cell delineation events

The following statistics are collected as 16 bit rollover counts for the UTOPIA interface:

- Receive buffer underflows
- Receive buffer overflows
- Receive interface protocol errors
- Transmit interface protocol errors
- Transmit parity errors

DCR Interface

The DCR interface provides a means to configure the Serial-UTOPIA Bridge, and read port and interface statistics. The DCR interface can be adapted easily to any standard microprocessor interface, and is directly available for MicroBlaze and PowerPC processors.

Core Modifications

Phystream provide a Xilinx NGC netlist to which modifications are not possible. Modifications to the core functionality can be undertaken, and may incur an additional charge.

Verification Methods

Extensive functional simulation has been performed at both the RTL and gate level using Modelsim 5.8.

Recommended Design Experience

The design team should have experience in HDL design for FPGAs.

Ordering Information

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