

Phystream Ltd

22 Elm Way, Melbourn,
 Royston, Herts
 United Kingdom, SG8 6UH
 Phone: +44 (0)20 8469 4019
 E-mail: query@phystream.com
 URL: www.phystream.com

Features

- Supports 1-16 physical TDM ports
- Clock, data and sync for connection to most DS1/E1 or DSL framers
- Programmable TDM frame formats
 - Independent transmit and receive
 - Sync pulse position
 - Frame length
 - TDM octet mapping within frame
 - Bit-level mapping
- Master and slave operation
 - Internal or external sync pulse
- Full timeslot discrimination
 - Supports superchannels
 - Supports subchannels
 - Configurable to desired channel density
- All ports fully independent

- Transmit and receive port sections fully independent
- Requires one clock buffer only

Core Facts

Provided with Core	
Documentation	User Guide
Design File Formats	Xilinx NGC netlist
Constraints Files	framer_if_wrapper.ucf
Verification	Test Bench, Test Vectors
Instantiation templates	VHDL, Verilog
Reference designs & application notes	
Additional Items	C Driver Code
Simulation Tool Used	
Modeltech Modelsim v5.8	
Support	
Support provided by Phystream Ltd	

- Reduced resource count for lesser port configurations
- C driver code available
- Available under terms of the SignOnce IP License
- Available on a range of target devices

Table 1: Example Implementation Statistics for 16-Port Configuration

Family	Example Device	Fmax (MHz)	Slices ¹	IOB ²	GCLK	BRAM	MULT	DCM/DLL	MGT	PPC	Design Tools
Spartan-3™	XC3S200-4	100	459	170	1	3	0	0	N/A	N/A	ISE 6.2.02i
Virtex-II Pro™	XC2VP2-7	100	468	170	1	3	0	0	0	0	ISE 6.2.02i
Virtex-II™	XC2V250-6	100	466	170	1	3	0	0	N/A	N/A	ISE 6.2.02i

Notes:

- 1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
- 2) Assumes 16-port configuration, core datapath signals are routed internally, serial and DCR interfaces are routed to device pins

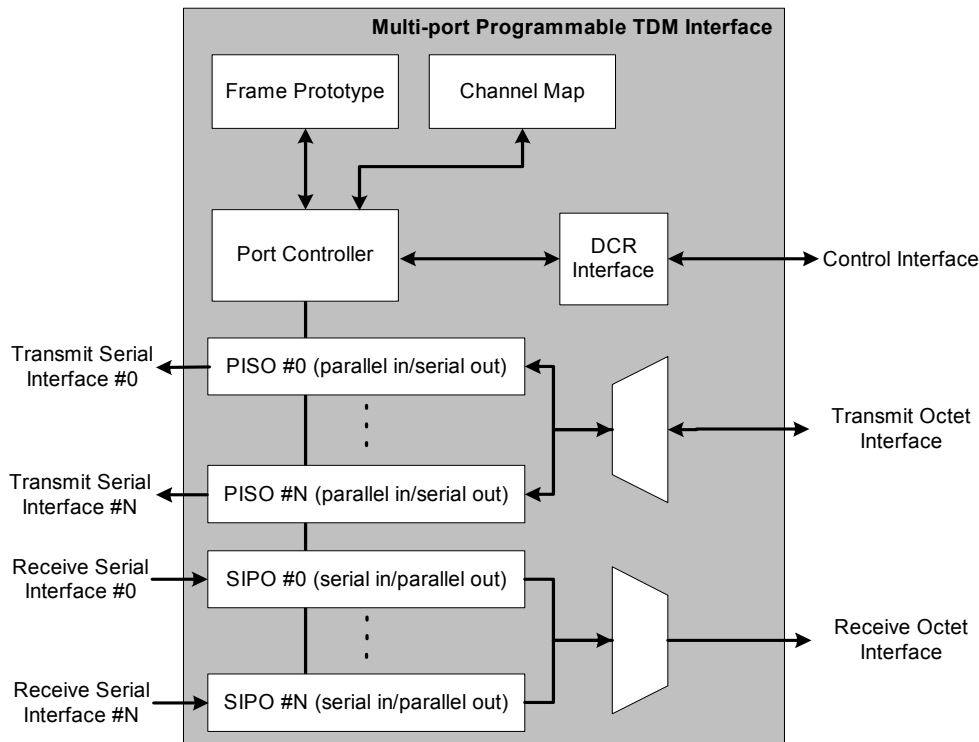


Figure 1: Multi-port Programmable TDM Interface Block Diagram

Applications

- Multi-service access platforms
- Integrated Access Devices (IADs)
- Standard Hardware platforms

General Description

The Multi-port TDM Interface provides flexible serial interfacing and timeslot mapping in an efficient, and easy to use IP block. It is suitable for port densities between 1 and 16 ports, operating at clock frequencies from 10MHz to 100MHz, depending on the required port density.

The Multi-port TDM Interface is suitable for direct connection to most DS1/E1 or DSL framers. The control interface allows each port, and port direction, to be configured for TDM frame format, channelization and interface functional timing.

The Multi-port TDM Interface provides a mapping for timeslot number, or even bit position within the TDM frame, to an internal channel identifier. This allows timeslot data to be mapped to superchannels or subchannels, with the channel identifier compressed for use by downstream datapath logic. Octets can be identified by a tributary identifier, or by a user-defined channel identifier, at the Octet Interface.

Functional Description

Port Controller

The Port Controller controls the transfer of data between the serial interfaces and the Octet Interface. The Port Controller polls each serial interface for a data bit transfer event. Once a bit has been transferred, the bit position within the TDM frame is looked up in a mapping table (Frame Prototype) in order to determine how to process that bit. The TDM format for each port direction is programmed through the

DCR Interface, allowing each port to be independently configured for E1, DS1, clear channel or proprietary frame formats. Received bits are accumulated in a holding register for transfer to the Octet Interface at the appropriate point within the TDM frame. The Port Controller synchronizes internal and external TDM frame phase as required.

The Port Controller maps each data word, 1-8 bits, to a channel identifier. The required channel density can be configured by instantiating a Channel Map memory of the required size. The mapping is provisionable through the DCR Interface.

Frame Prototype

The Frame Prototype contains the mapping between the TDM frame format and Octet Interface. In addition it specifies the TDM port functional timing. The mapping indicates which bits are to be accepted, and when to transfer data bits between the Serial Interfaces and Octet Interface. The transfer can be made for less than 8 bits, allowing subchannels to be supported. The TDM port functional timing specifies the position of the frame synchronization pulse within the TDM frame, and the length of the TDM frame.

Channel Map

The Channel Map provides the mapping between data words at the Serial Interface, and internal channel identifiers. In this way superchannels are supported, allowing a number of timeslots to be associated with a single identifier. Each valid data word at the Octet Interface is presented with the associated tributary identifier and channel identifier.

DCR Interface

The DCR (Device Control Register) bus is part of the IBM CoreConnect™ standard for on-chip bus communication. This interface provides a means to configure the TDM Prototype and Channel Map. The DCR interface can be adapted easily to any standard microprocessor interface, and is supported directly on PowerPC and MicroBlaze.

Core Modifications

Phystream provide a Xilinx NGC netlist to which modifications are not possible. The Channel Map, however, is supplied as a separate NGO file, so that the user can customize the channel density. The core can be supplied configured for a specific number of ports 1-16, and for the required channel density. Further modifications to the core functionality can be undertaken.

Verification Methods

Extensive functional simulation has been performed at both the RTL and gate level using Modelsim 5.8.

Recommended Design Experience

The design team should have experience in HDL design for FPGAs.

Ordering Information

This product is available directly from Phystream under the terms of the SignOnce IP License. Please contact Phystream for pricing and additional information about this product. Contact information for them is on the front page of this datasheet. To learn more about the SignOnce IP License program, contact Phystream or visit the web:

Email: commonlicense@xilinx.com
URL: www.xilinx.com/ipcenter/signonce

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com