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Features

- UTOPIA Level 2 PHY interface
 - Conforms to af-phy-0039.000
 - Cell or octet-level handshake
 - 8-bit data
- Transmit cell rate enforcer
 - Controls up to 31 independent PHY ports
 - Programmable divider with 24-bit precision
- Receive cell rate generator
 - Controls up to 31 independent PHY ports
 - Programmable divider with 24-bit precision
- Optimized for use with Phystream phyCore Dataflow Processor
- DCR (Device Control Register) configuration interface
- Available under terms of the SignOnce IP License

Core Facts	
Provided with Core	
Documentation	User Guide
Design File Formats	Xilinx NGC netlist
Constraints Files	atmtc.ucf
Verification	Test Bench, Test Vectors
Instantiation templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
Modeltech modelsim 5.7g	
Support	
Support provided by Phystream Limited	

Table 1: Example Implementation Statistics for ATMTC (64 links)

Family	Example Device	Fmax (MHz)	Slices ¹	IOB ²	GCLK ³	BRAM	MULT	DCM/DLL	MGT	PPC	Design Tools
Spartan-3™	XC3S400-4	100	940	36	4	0	0	0	N/A	N/A	ISE 6.2.03i
Virtex-II Pro™	XC2VP4-5	100	968	36	4	0	0	0	0	0	ISE 6.2.03i

Notes:

- 1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
- 2) Assuming UTOPIA interface signals only routed off-chip
- 3) Assuming independent system, DCR, UTOPIA transmit and UTOPIA receive clocks

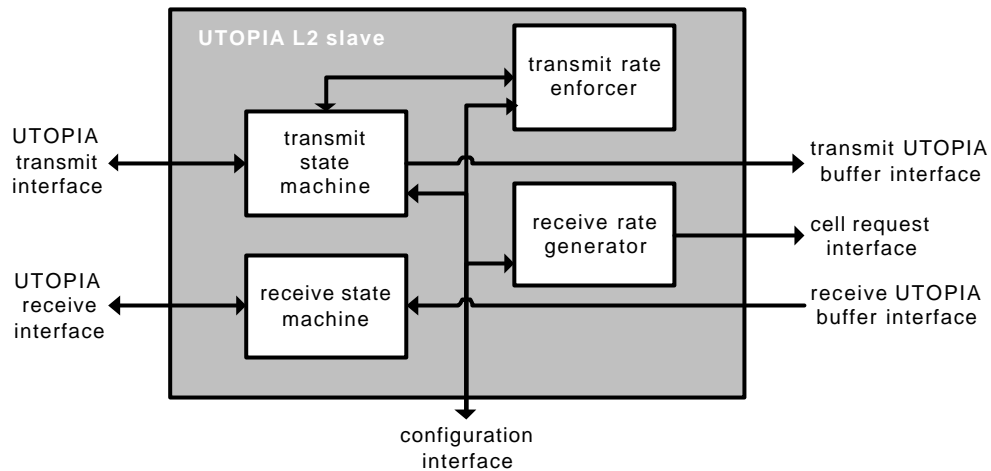


Figure 1: UTOPIA Level 2 Slave for phyCore Block Diagram

Applications

The Phystream UTOPIA level 2 is designed primarily for internal interconnect, rather than as a direct interface for a physical layer device. The implication is that flow control is not based on the buffer fill level of a physical port FIFO. Rather, the cell rate for each PHY can be programmed. It is assumed that there is additional buffering and buffer management between the UTOPIA interface and line interface. In particular, the UTOPIA level 2 interface is designed as a peripheral for the Phystream phyCore Dataflow Processor. phyCore is a generic data processing platform, which can be used for the development of a wide range of applications, including ATM cell processing:

- Circuit Emulation Service (AAL1)
- Voice Transport over ATM (AAL2)
- Packet Inter-working (AAL5)

General Description

The UTOPIA level 2 slave interface provides standard cell or octet level handshaking as specified by af-phy-0064.000. The interface is intended for point-to-point connection. The module acts as a PHY interface. A programmable rate controller controls the flow of cells in each direction. The required inter-cell interval can be programmed for each PHY port, in each direction, over the Device Control Register (DCR) control interface.

Functional Description

Transmit State Machine

The Transmit State Machine performs octet or cell level handshaking to control the transfer of cells from a mating ATM layer interface. The module can be built to check and discard the ATM HEC, or pass the HEC transparently. The state machine can also be built to filter unassigned cells.

The state machine is robust in the presence of errors. A watchdog timer prevents the interface from locking up in the presence of protocol errors, as may occur when either the ATM or PHY sides of the interface are reset independently.

The Transmit State Machine maintains the status of the downstream Transmit UTOPIA buffer, which is not part of the core. Cell writes are signalled downstream, whilst cell reads are received from downstream. The Transmit UTOPIA buffer is organized as a single FIFO buffer, containing up to 32 cells. This provides more

efficient use of available memory than a fixed buffer allocation when there are disparate PHY cell rates. The originating PHY address is appended to each cell in order to identify cells through the Transmit UTOPIA Buffer.

Each Transmit PHY port has an associated enable that can be programmed through the DCR control interface.

The Transmit State Machine decodes the following events, which can be used to drive interface statistics counters or generate interrupts:

- Transmit Parity Error
- Transmit Interface Protocol Error (watchdog timeout)
- Transmit UTOPIA Buffer Overflow
- Transmit HEC Error

Transmit Rate Enforcer

The Transmit Rate Enforcer generates the cell available (*clav*) signals for each transmit PHY port. The *clav* signal is asserted at a programmed inter-cell interval. The inter-cell interval is specified as a fractional division of the system clock frequency, with 24-bit accuracy. An inter-cell interval can be programmed for each PHY port through the DCR control interface.

Receive State Machine

The Receive State Machine performs octet or cell level handshaking to control the transfer of cells to a mating ATM layer interface. The module can be built to calculate and insert the ATM HEC, or pass the HEC transparently. The interface is only intended for point to point (single PHY device, multiple PHY port) operation.

The Receive State Machine maintains the status of the upstream Receive UTOPIA buffer, which is not part of the core. Cell reads are signalled upstream, whilst cell writes are received from upstream. The Receive UTOPIA buffer is organized as a single FIFO buffer. This provides more efficient use of available memory when there are disparate PHY cell rates. The originating PHY address is appended to each cell in order to identify cells through the Receive UTOPIA Buffer. The PHY address of the cell at the head of the Receive UTOPIA Buffer FIFO is used to respond to ATM layer polling. If the ATM layer selects any other address a polling error is deemed to have occurred, and is signalled by an event output.

The Receive State Machine decodes the following events, which can be used to drive interface statistics counters or generate interrupts:

- Receive UTOPIA Buffer Overflow
- Receive UTOPIA Buffer Underflow
- Receive UTOPIA Polling Error (selected address does not requested address)

Receive Rate Generator

The Receive Rate Generator generates cell requests for each receive PHY port at a programmed inter-cell interval. The inter-cell interval is specified as a fractional division of the system clock frequency, with 24-bit accuracy. An inter-cell interval can be programmed for each PHY port through the DCR control interface.

The cell requests specify as a pair of queue identifiers that are compatible with phyCore, Phystream's Dataflow Processor. The form is a pair of 16 bit numbers, which represent a buffer source and buffer return queue. The source queues have a one to one correspondence with UTOPIA PHY ports, and so the requesting port can be easily determined in applications not using phyCore.

Core Modifications

The UTOPIA Level 2 Slave for phyCore module is supplied as a Xilinx NGC netlist. Verilog source code can be purchased for user customization. Alternatively, Phystream can undertake customization of the core as required.

Verification Methods

The UTOPIA module has been tested in simulation using modelsim 5.7g, and on a Virtex-E development platform.

Recommended Design Experience

Knowledge of HDL design and Xilinx tools is recommended for use of this core. Knowledge of ATM systems would also be useful.

Available Support Products

The UTOPIA Slave for phyCore module is designed primarily for use with Phystream's phyCore Dataflow Processor. A range of hardware and software modules, including interfaces, hardware acceleration and application software, can be combined to address a wide range of ATM processing tasks, including traffic management and OAM processing.

Ordering Information

This product is available directly from Phystream under the terms of the SignOnce IP License. Please contact Phystream for pricing and additional information about this product. Contact information for Phystream is on the front page of this datasheet. To learn more about the SignOnce IP License program, contact Phystream or visit the web:

Email: commonlicense@xilinx.com
URL: www.xilinx.com/ipcenter/signonce

Related Information

Industry Information

The following specifications are available from The ATM Forum at www.atmforum.com:

- UTOPIA Level 2, version 1.0 af-phy-0039.000

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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